

**The paragraph beginning at page 14, line 16, has been replaced with the following,
rewritten paragraph:**

A3 -- Next, in step of FIG. 9B, and SiN film is deposited on the GaAs substrate **61** by plasma CVD process such that the SiN film covers the WSi gate electrode **63**, and side wall insulation films **63A** and **63B** are formed on both lateral side walls of the gate electrode **63** as a result of anisotropic etching process applied of the SiN film such that the etching proceeds generally perpendicular to the principal surface of the substrate **61**. --

**The paragraph beginning at page 14, line 25 has been replaced with the following,
rewritten paragraph:**

A4 -- In the step of FIG. 9B, a further ion implantation process of Si⁺ is conducted under an acceleration voltage of 50keV with a dose of 5 x 10cm⁻² while using WSi gate electrode **63** and the side wall insulation films **63A** and **63B** as a self-aligned mask, and n⁺-type diffusion regions **61D** and **61E** are formed in the GaAs substrate **61** at outer sides of the LDD regions **61B** and **61C**, respectively. --

IN THE CLAIMS:

Please amend Claim 1, as follows:

- A5 1. (Amended) A semiconductor triode, comprising:
- a compound semiconductor layer including a channel layer;
 - a first ohmic electrode supplying carriers into said channel layer;
 - a second ohmic electrode collecting carriers from said channel layer; and